Jitter effects on Analog to Digital and Digital to Analog Converters

Jitter

One of the significant problems in digital audio is clock jitter and its impact on a signal integrity in audio chain. While many believe that clock jitter impacts all digital audio signals, it is my contention that clock jitter affects the signal only during the conversion process. Analog to digital and digital to analog converters are susceptible to clock jitter and can exhibit degraded performance with even small amounts of jitter. Beyond this realm the fundamental tenants of digital clocking render small variations in clock transition times relatively harmless, that is until they begin to fall outside clock-data setup and hold times.

How much is too much jitter? For a 24 bit quantized signal jitter greater than 3 – 5 pico-seconds can measurably degrade the performance of a converter. While this seems like a very small amount (it is) many of today's products provide systems with clock jitter approaching this range. Another point to consider is that most 24-bit converters actually operate in the theoretical 18 - 20 bit range thus relaxing, by a small amount, the need for increasingly smaller jitter amplitudes.

What Is Clock Jitter?

Digital circuits operate from a master clock that is used to derive sequencing and control the work or computations they are designed for. In digital audio these clocks are part of the analog to digital (ADC) and digital to analog (DAC) conversion process. These clocks are typically not perfect with respect to their

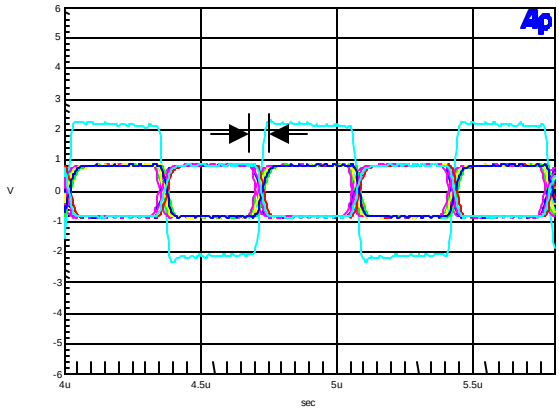

Figure 1 Transition edges showing jitter

transitions and will display minute variations over time. Figure 1 shows a graph of multiple clock transitions superimposed over time (called an eye pattern). Note how the transition edges do not all coincide with each other but cause a fairly wide band at each transition point. This is (one form of) jitter, a relatively large amount of jitter, caused by noise in the oscillator circuitry of an inexpensive function generator.

The analog to digital process relies upon a sample clock to indicate when a sample or snap shot of the analog signal will be taken. In order to accurately represent the analog data the sample clock must be evenly spaced in time. Any deviation will result in a distortion of the digitization process. Note too that the sensitivity to variations in the sampling interval is greatest during the times when the analog signal has the greatest change in voltage with respect to time. For example, in figure 2, assume the vertical lines, spaced at 2uSec intervals are the sample times. A small deviation of the sample clock at the negative peak (red line) of the sine wave will yield a smaller error signal or difference in the sample value than a similar variation at the rising or falling edge of the sine wave. The difference between the two sample points at the rising edge of the sine wave yields a significantly different value in the sampled data. We can conclude that a given amount of clock jitter has a greater effect as the signal amplitude and frequency increase since in both cases the change in unit time of the signal is greater with high level, high frequency signals. Therefor jitter has less effect on low level, low frequency signals, and more affect on high level, high frequency signals.

It's important to note that jitter in the sample clock is detrimental since once an analog signal is converted it's virtually impossible recreate the small timing variations in such a way as to reassemble the digital signal back to analog in its original form. If one had a perfect ADC and a perfect DAC and used the same clock to drive both units, then, (and ignoring certain other factors), there would be no impact on the signal from jitter. In a real world system a digitized signal travels through multiple processors, usually parks itself on a disk or piece of tape for a while and then goes through more processing before conversion back to analog. Thus, the clock pulses used to convert the signal have long since gone and are replaced with newer ones with their own subtle variations.

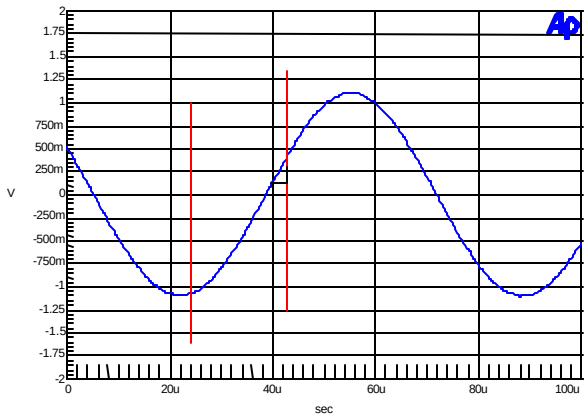

Figure 2 – sample intervals

From the perspective of converting analog signals to digital or digital signals to analog, there are two basic clock sources we should consider. One, the internal clock, present in most ADCs, is usually derived from a crystal oscillator. The second is an external clock source, in the form of a word clock, AES or S/PDIF signal that is used to synchronize multiple devices to one clock or to carry clocking and digital data for conversion back to analog.

Internal clocks are usually very stable with respect to frequency and jitter and unless the circuits are noisy or poorly designed, jitter on the order of 3 to 10pS is possible. An analog to digital converter using such an internal clock will usually yield the best performance with respect to jitter effects.

External clocking modes require a converter to regenerate its internal clocks from an external clock. Since the converter is likely to need several frequency multiples of the external word clock a phase locked loop is used to generate these clocks. The new clocks will be multiples of the external clock and will be used to drive the actual conversion process. This regeneration process can introduce jitter into the sample clock in several ways and great care must be taken in the phase locked loop design to manage intrinsic phase noise and control the amount of interference from other circuitry in the system. The bottom line is that although many good converters will exhibit very low jitter in their phase locked loops, the internal clock source will often provide slightly better performance with respect to jitter.

For digital to analog conversion the sample clock is usually derived from an AES or S/PDIf bit stream. And like the analog to digital converter, this regeneration process can introduce jitter into the sample clock in the same ways. There are schemes used to reduce jitter in regenerated clocks and some are very good. In the long run it comes down to good circuit design practices to maintain performance as close to theoretical as possible.

To add a bit of complexity to our thinking, jitter can have different probability distributions depending on the source. We'll look at three and show what their effects are on sampled signals. Sine and square wave induced jitter is common and results from the pickup of the analog signals to be converted, the digital

representation of the analog signal following conversion and from direct and indirect effects of the conversion sample clocks. Less easy to detect is jitter caused by wide band noise that generates a random distribution and manifests as increased noise and distortion in the audio signal. So, the sources of the jitter have an effect on its distribution and in turn an effect on the disturbance to the audio signal.

Effects of Clock Jitter

Figure 3 shows an FFT of a 15kHz sine wave being converted from the analog domain to the digital domain. There is little or no jitter present and the signal presents a pure spike at the signal frequency.

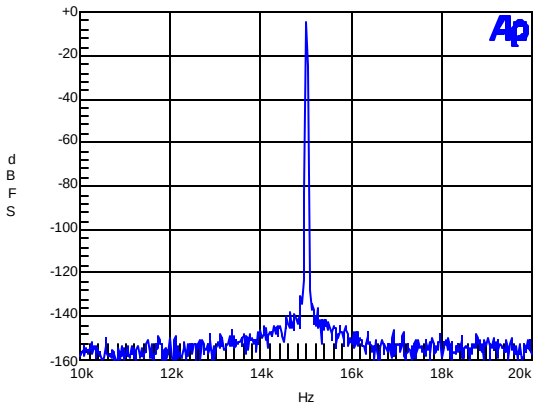

Figure 3
Low jitter ADC FFT

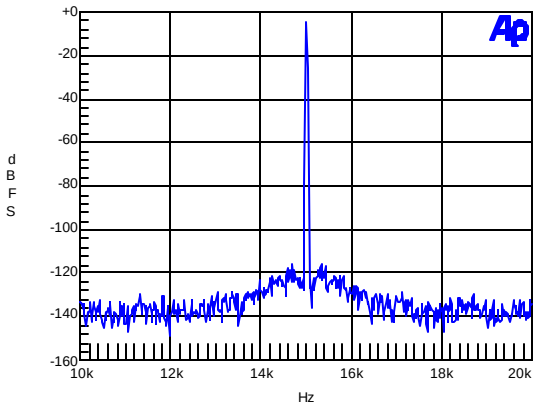

Figure 4
1 nSec broadband jitter

Using test equipment designed to generate jitter one can see the effects of injecting 1 nano-second jitter with a random distribution in figure 4. The jitter affects the entire audio spectrum and has its greatest affect on the noise floor. One can see an approximate increase in the FFT noise floor of 20dB. This may be the least obnoxious jitter since its affect is generally distributed over the entire audio range and is therefore less likely to be noticed as anything more than noise.

When the jitter is caused by coherent noise in the system, the results are often more noticeable. For example, figure 5 shows the effect of a 1kHz jitter signal at 1nSec. Here one can see side lobes off the main signal that fall 1kHz from the signal being converted. These side lobes actually represent energy taken from the fundamental frequency and redistributed in the frequency domain.

Aurally the effects of this type of jitter can be quite harsh even though the side lobe amplitudes are approximately 120dB below the full-scale signal. Since they will have no musical relationship to the signal they will typically be audible as long as other masking agents do not interfere. Taking things a step further, if the generation of clock jitter is induced by a square wave the resultant effect will include harmonic multiples of the jitter frequency in the audio signal. Figure 6 shows the effect of square wave jitter causing multiple side lobes, harmonically related to the clock disturbance, but dissonant to the content of the audio signal.

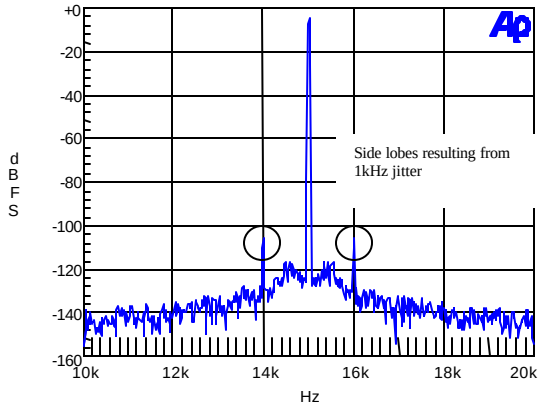

Figure 5
1 nSec Sine jitter 1kHz

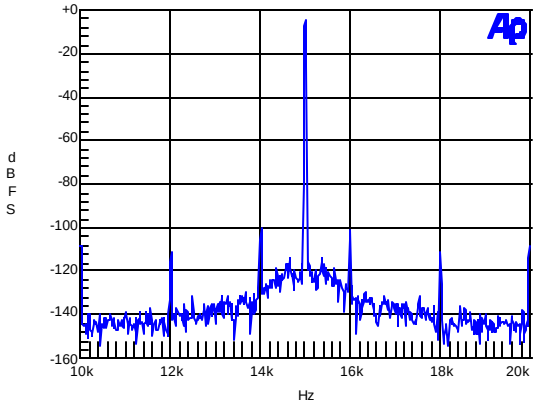

Figure 6
1 nSec square wave jitter 1kHz

These FFT's show how the various jitter types manifest in an analog to digital converter. The effects indicate an increase in the noise floor when wide-band jitter is introduced and the presence of coherent tones spaced at intervals of the jitter frequency when narrow band noise is introduced. It should be noted that jitter is present only when a signal is present and that the anomalies shown above are not there in the absence of an input signal. This is due to the fact that the attendant noises and side lobes caused by jitter are derived from the input signal itself and obtain energy from those signals. Further, the effects of jitter are magnified as the input signal increases in both frequency and amplitude. 1 nano-second of jitter will have a far greater impact on a 10kHz full-scale signal than a 100Hz full-scale signal. To intuitively grasp the relationship between jitter, frequency and amplitude refer to our discussion around figure 2.

What this all means from a listening perspective depends on the musical signal being converted and the type of jitter in the system. As we saw earlier, jitter caused by coherent signals will result in non-harmonically related noise in the system and may be readily perceived as a harsh, edgy sound when listening. Note that while the wide-band jitter appears to be the least objectionable the measurements shown in figures 7 and 8 illustrate that all jitter increases the amount of measurable THD in the system.

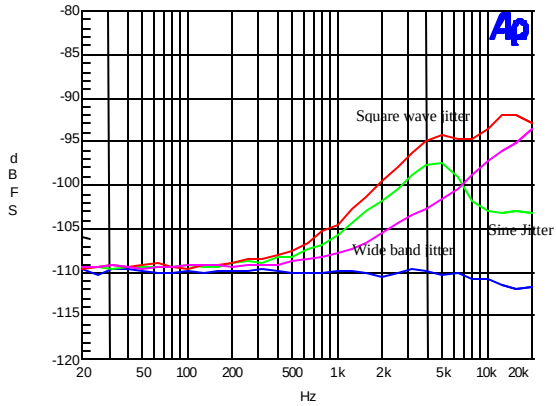

Figure 7
ADC THD with various jitter

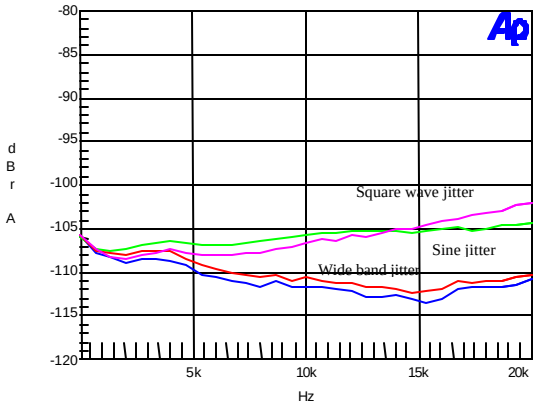

Figure 8
DAC THD with various Jitter

Figure 7 shows the effects one might see on THD from different jitter sources in an analog to digital converter. The overall effect is an increase in THD in the high frequencies. Since all three jitter sources have similar results on THD and noise measurements it is instructive to be able to view an FFT of the signal under test (preferably a high frequency, high amplitude signal) to see if there are enharmonic noise spikes resulting from the signal input.

The graph in figure 8 shows the jitter effects on THD and noise for a digital to analog converter. Here the results are similar to the analog to digital conversion with an attendant rise in high frequency THD. Note that the wide-band jitter has less effect on the DACs output (than the ADC) due to the system's ability to filter out this type of jitter.

It is possible to configure a test setup using a high quality analog to digital converter after the DAC under test to provide FFTs of the DAC's analog output signal. By injecting jitter into the digital output signal feeding the DAC and requantizing the DAC's analog output, similar anomalies can be viewed in the DAC's FFT. Figure 9 shows the same DAC (in figure 8) with no jitter, figure 10 shows the effect of wide-band jitter and figures 11 and 12 with sine and square wave jitter applied to the digital input of the DAC. As with analog to digital conversion, similar characteristics are visible in these plots.

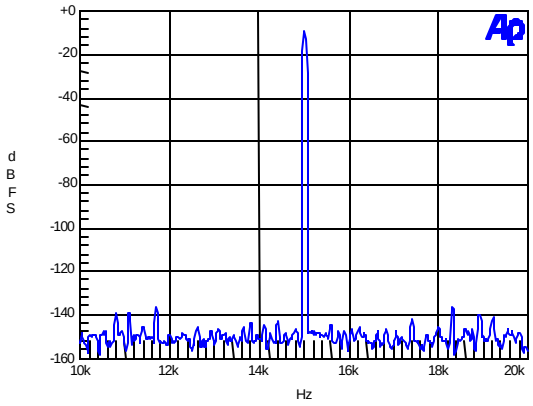

Figure 9
DAC output with no added jitter

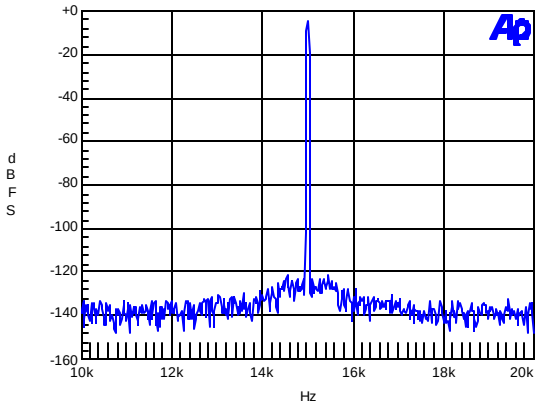

Figure 10
DAC output with 1 nSec wide band jitter

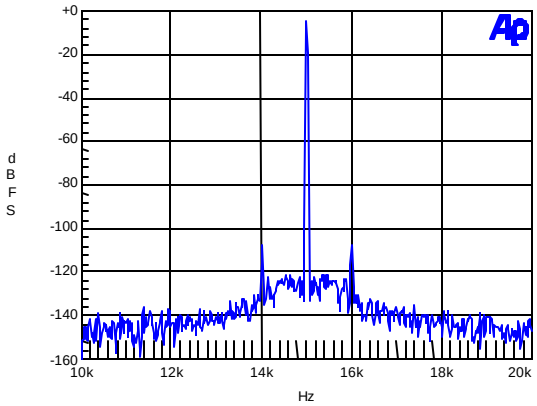

Figure 11
DAC output with 1 nSec Sine Jitter 1kHz

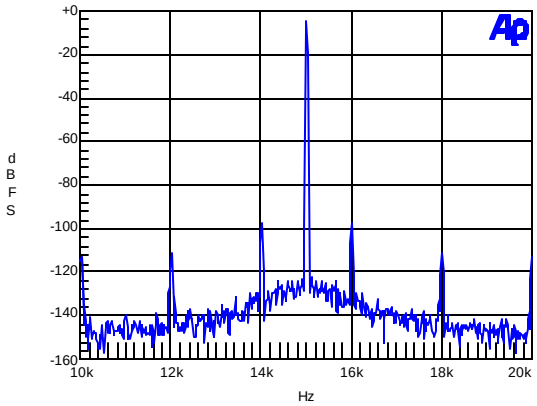

Figure 12
DAC output with 1 nSec square wave jitter 1kHz

Conclusion

In conclusion, the following observations are important relative to jitter when working with analog to digital or digital to analog conversions.

1. Analog to digital converters are typically less prone to jitter effects if the internal clock modes are used.
2. Once a signal has undergone a conversion (analog to digital), there is little, if anything, one can do to correct the effects of jitter on the converted signal.
3. Jitter affects the higher frequencies more than lower frequencies and affects higher signal amplitudes more than lower signal amplitudes. The most susceptible signals are near full-scale, high frequency signals.
4. Jitter can be caused by intrinsic circuit problems as well as external sources and is usually a combination of the two. It is necessary to make certain that external clocks used for synchronizing analog to digital converters or signals carrying data to digital to analog converters are properly terminated, are not modified or disturbed by the delivery medium (cable inductance & capacitance) and are not subject to high noise environments.
5. The effect jitter has on the conversion process is dependant on the nature of the jitter and its amplitude. 50pSec of jitter will have less effect on a signal than 500pSec. Jitter that has a wide-band distribution characteristic will usually sound less offensive than jitter that has a defined, coherent distribution.

